LEAKAGE CURRENT REDUCTION METHOD

FIELD OF THE INVENTION

The present invention relates to electronic circuitry and, in particular, to a leakage current reduction method.

BACKGROUND OF THE INVENTION

In a prior approach for powering down a circuit system, when the system goes into sleep / data retention mode, the main power supply VDD goes from 1.3V (in active mode) to near 0V, a retaining power supply VRET remains unchanged at, for example, 1.3V, a retain signal RET goes from 0V to VRET (1.3V) level, and some internal nodes of the system are raised to a reference voltage VBB level (for example 0.6V).

For circuits whose data needs to be retained when the system goes into sleep / data retention mode, the typical way of turning off the P Channel (PCH) device is shown below:

Vdrain = VBB (0V --> 0.6V, for example)
Vgate = RET (0 --> 1.3V, for example)
Vsource = VDD (1.3V --> 0V, for example)
Vbulk = VRET (1.3V , for example)